F I G. 1

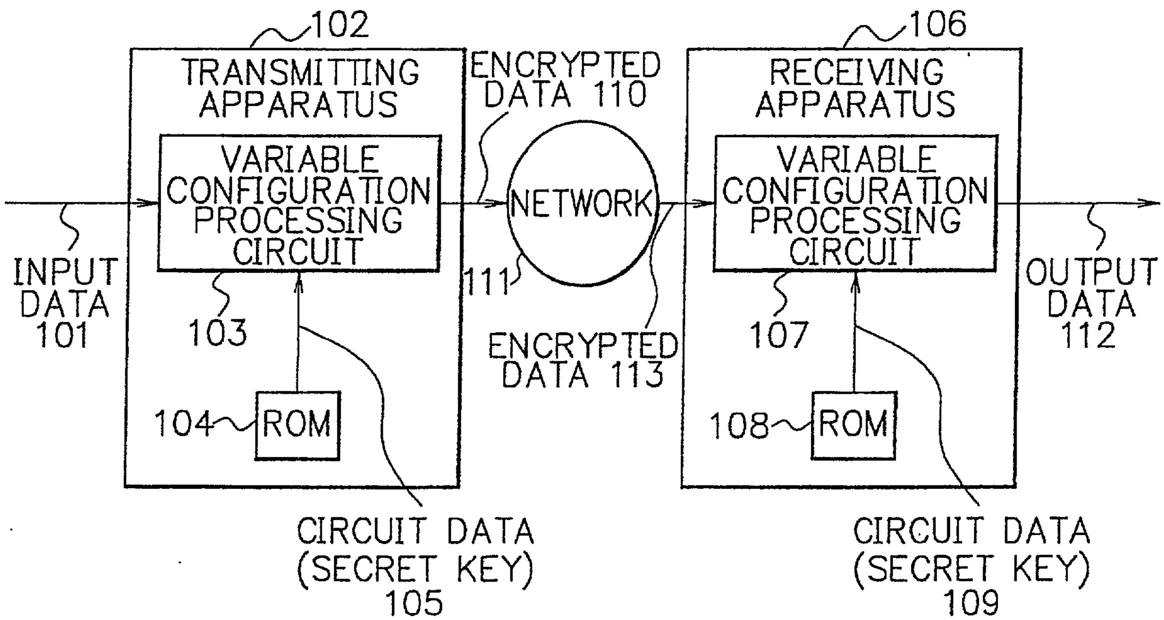

102
TRANSMITTING APPARATUS
VARIABLE CONFIGURATION PROCESSING CIRCUIT
103
104
ROM
INPUT DATA 101
ENCRYPTED DATA 110
NETWORK
111
ENCRYPTED DATA 113
CIRCUIT DATA (SECRET KEY) 105
106
RECEIVING APPARATUS
VARIABLE CONFIGURATION PROCESSING CIRCUIT
107
108
ROM
OUTPUT DATA 112
CIRCUIT DATA (SECRET KEY) 109

FIG. 2

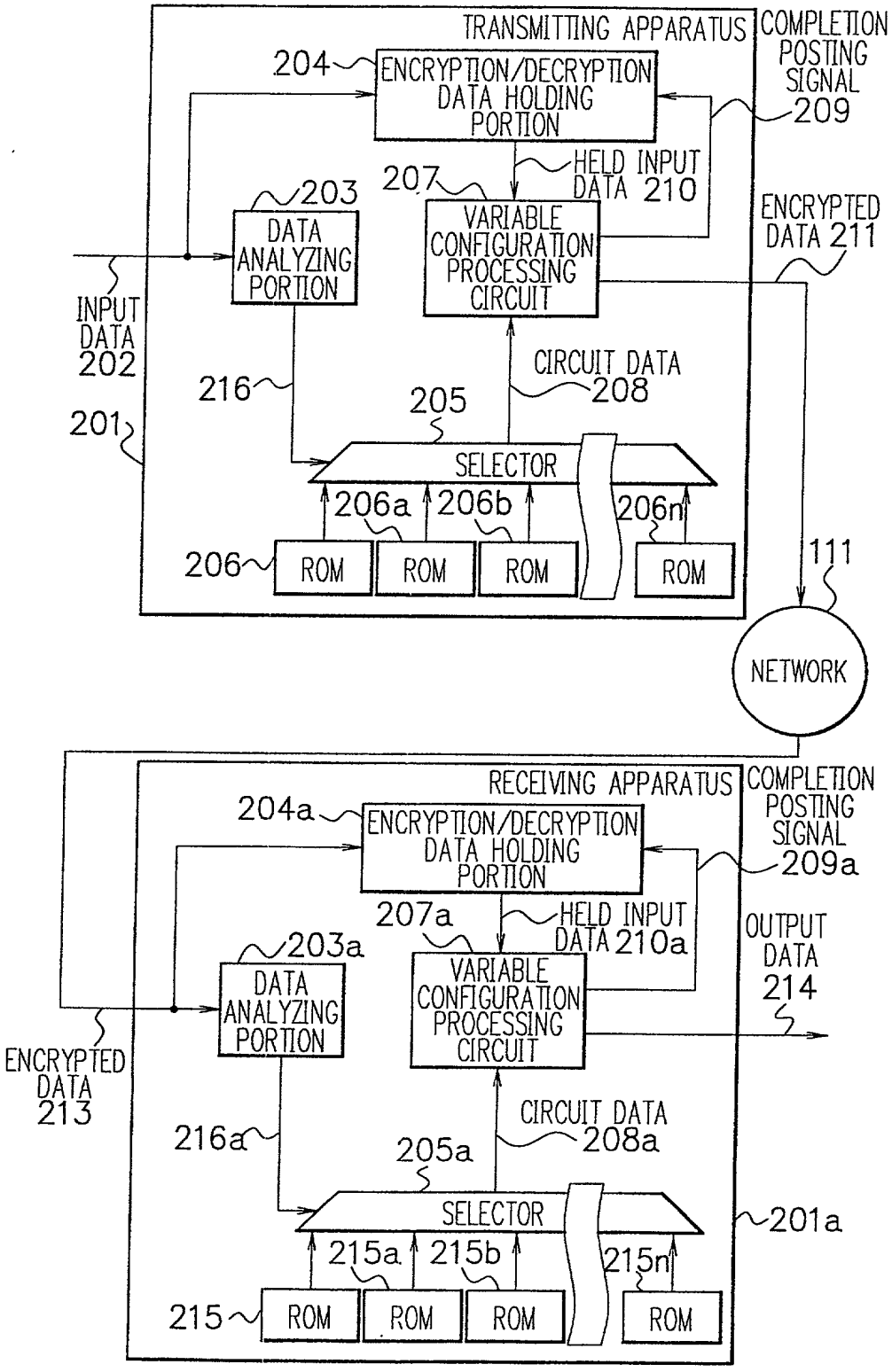

TRANSMITTING APPARATUS
COMPLETION POSTING SIGNAL 209
204
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
HELD INPUT DATA 210
207
203
DATA ANALYZING PORTION
VARIABLE CONFIGURATION PROCESSING CIRCUIT
ENCRYPTED DATA 211
INPUT DATA 202
CIRCUIT DATA 208
216
205
201
SELECTOR
206a
206b
206n
206
ROM
ROM
ROM
ROM
111
NETWORK
RECEIVING APPARATUS
COMPLETION POSTING SIGNAL 209a
204a
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
207a
HELD INPUT DATA 210a
OUTPUT DATA 214
203a
DATA ANALYZING PORTION
VARIABLE CONFIGURATION PROCESSING CIRCUIT
ENCRYPTED DATA 213
CIRCUIT DATA 208a
216a
205a
SELECTOR
201a
215a
215b
215n
215
ROM
ROM
ROM
ROM

FIG. 3

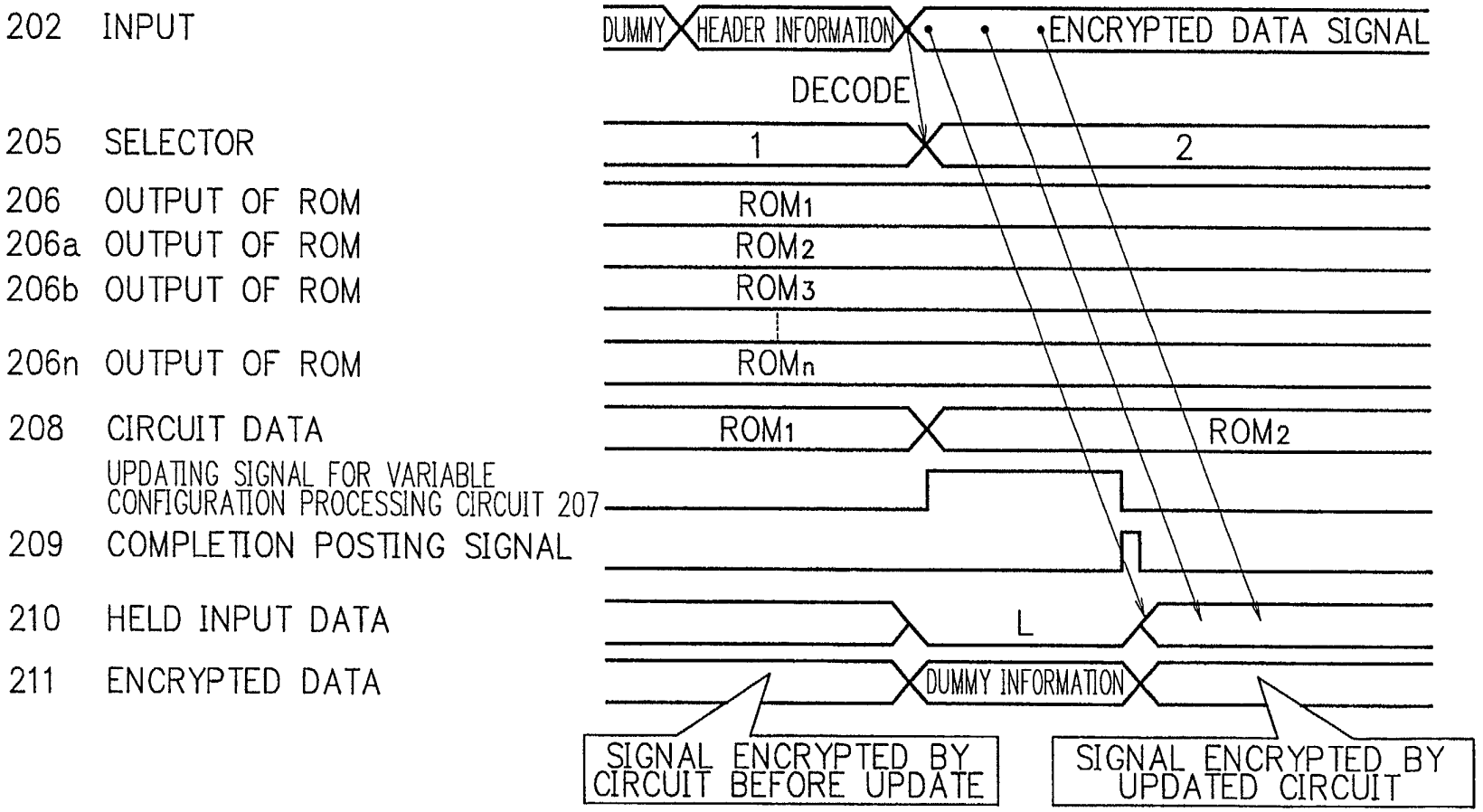


FIG. 4

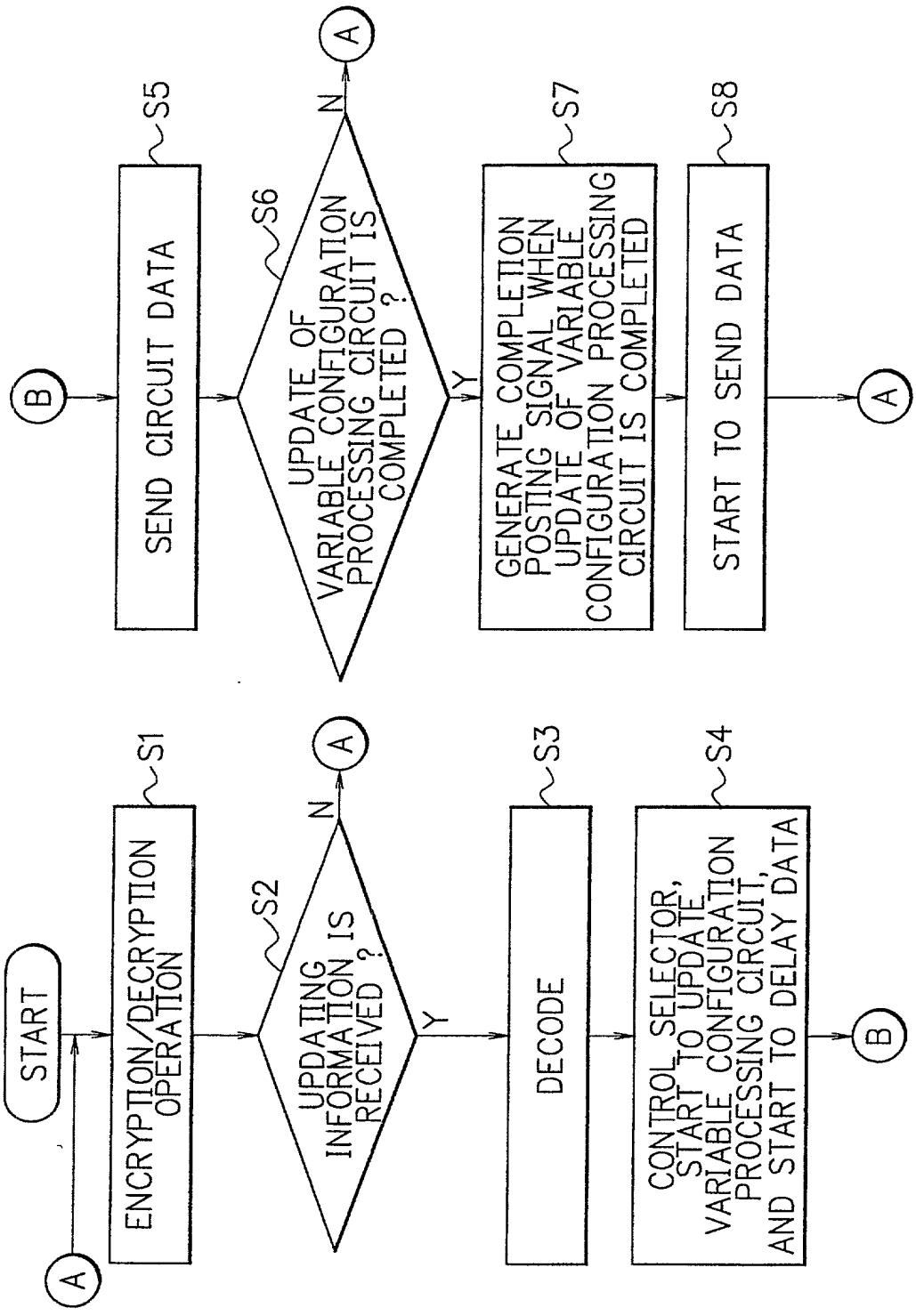

START
A
ENCRYPTION/DECRYPTION OPERATION
S1
UPDATING INFORMATION IS RECEIVED ?
S2
N
A
Y
DECODE
S3
CONTROL SELECTOR, START TO UPDATE VARIABLE CONFIGURATION PROCESSING CIRCUIT, AND START TO DELAY DATA
S4
B
B
SEND CIRCUIT DATA
S5
UPDATE OF VARIABLE CONFIGURATION PROCESSING CIRCUIT IS COMPLETED ?
S6
N
A
Y
GENERATE COMPLETION POSTING SIGNAL WHEN UPDATE OF VARIABLE CONFIGURATION PROCESSING CIRCUIT IS COMPLETED
S7
START TO SEND DATA
S8
A

FIG. 5

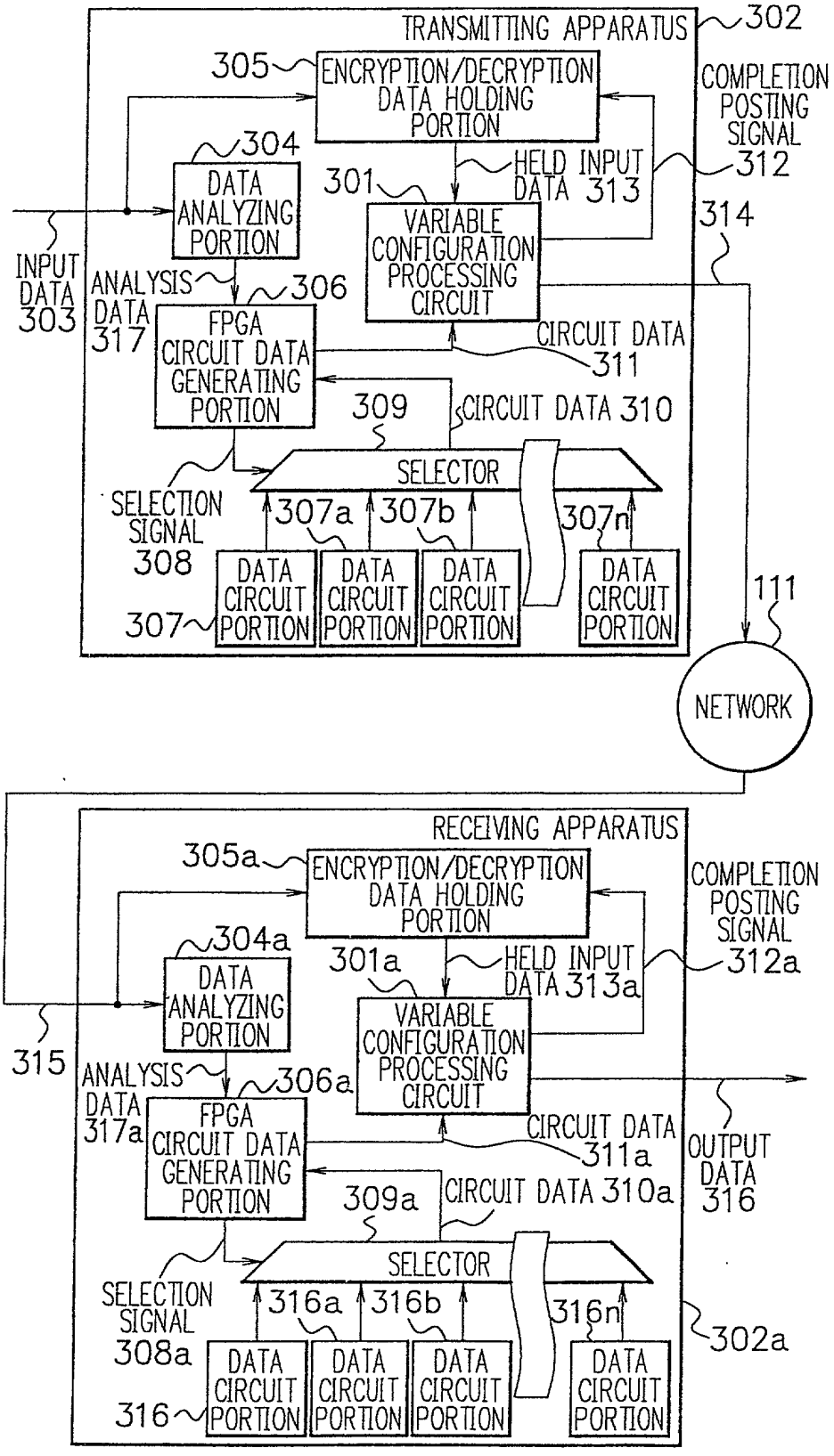

TRANSMITTING APPARATUS
302
305
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
COMPLETION POSTING SIGNAL
312
304
DATA ANALYZING PORTION
301
HELD INPUT DATA 313
VARIABLE CONFIGURATION PROCESSING CIRCUIT
314
INPUT DATA 303
ANALYSIS DATA 317
306
FPGA CIRCUIT DATA GENERATING PORTION
CIRCUIT DATA 311
309
CIRCUIT DATA 310
SELECTOR
SELECTION SIGNAL 308
307a
307b
307n
DATA CIRCUIT PORTION
307
111
NETWORK
RECEIVING APPARATUS
305a
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
COMPLETION POSTING SIGNAL
312a
304a
DATA ANALYZING PORTION
301a
HELD INPUT DATA 313a
VARIABLE CONFIGURATION PROCESSING CIRCUIT
315
ANALYSIS DATA 317a
306a
FPGA CIRCUIT DATA GENERATING PORTION
CIRCUIT DATA 311a
OUTPUT DATA 316
309a
CIRCUIT DATA 310a
SELECTOR
SELECTION SIGNAL 308a
316a
316b
316n
302a
DATA CIRCUIT PORTION
316

FIG. 6

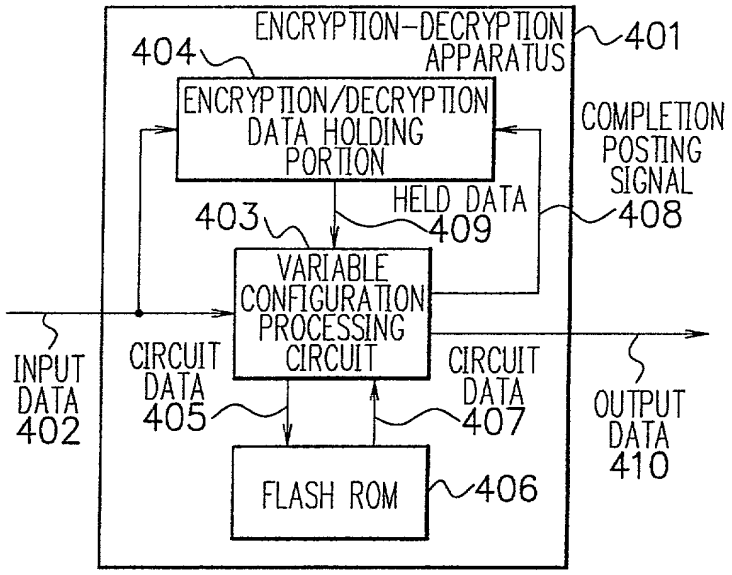

ENCRYPTION-DECRYPTION APPARATUS
401
404
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
COMPLETION POSTING SIGNAL
408
HELD DATA
409
403
VARIABLE CONFIGURATION PROCESSING CIRCUIT
INPUT DATA
402
CIRCUIT DATA
405
CIRCUIT DATA
407
OUTPUT DATA
410
FLASH ROM
406

FIG. 7

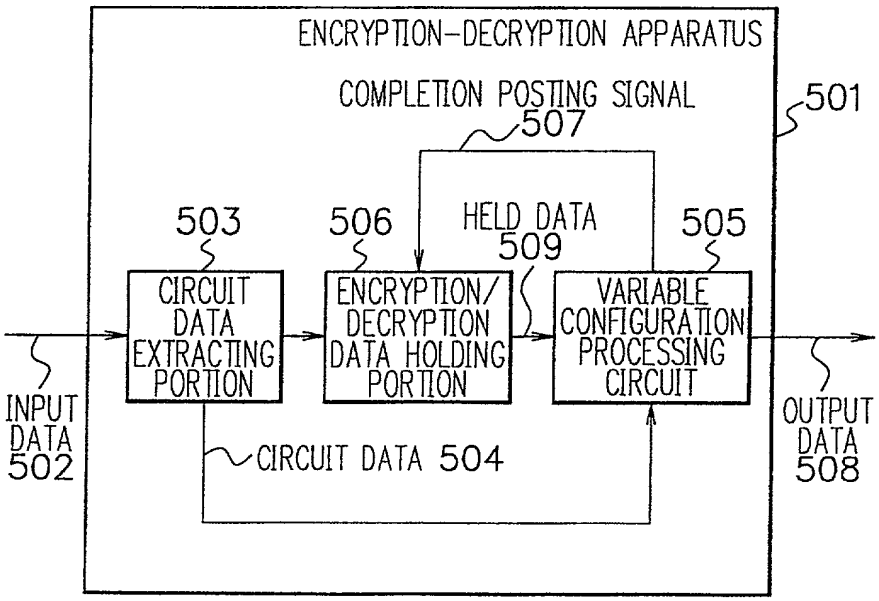

ENCRYPTION-DECRYPTION APPARATUS
COMPLETION POSTING SIGNAL
507
501
503
506
HELD DATA
509
505
CIRCUIT DATA EXTRACTING PORTION
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
VARIABLE CONFIGURATION PROCESSING CIRCUIT
INPUT DATA
502
CIRCUIT DATA 504
OUTPUT DATA
508

FIG. 8

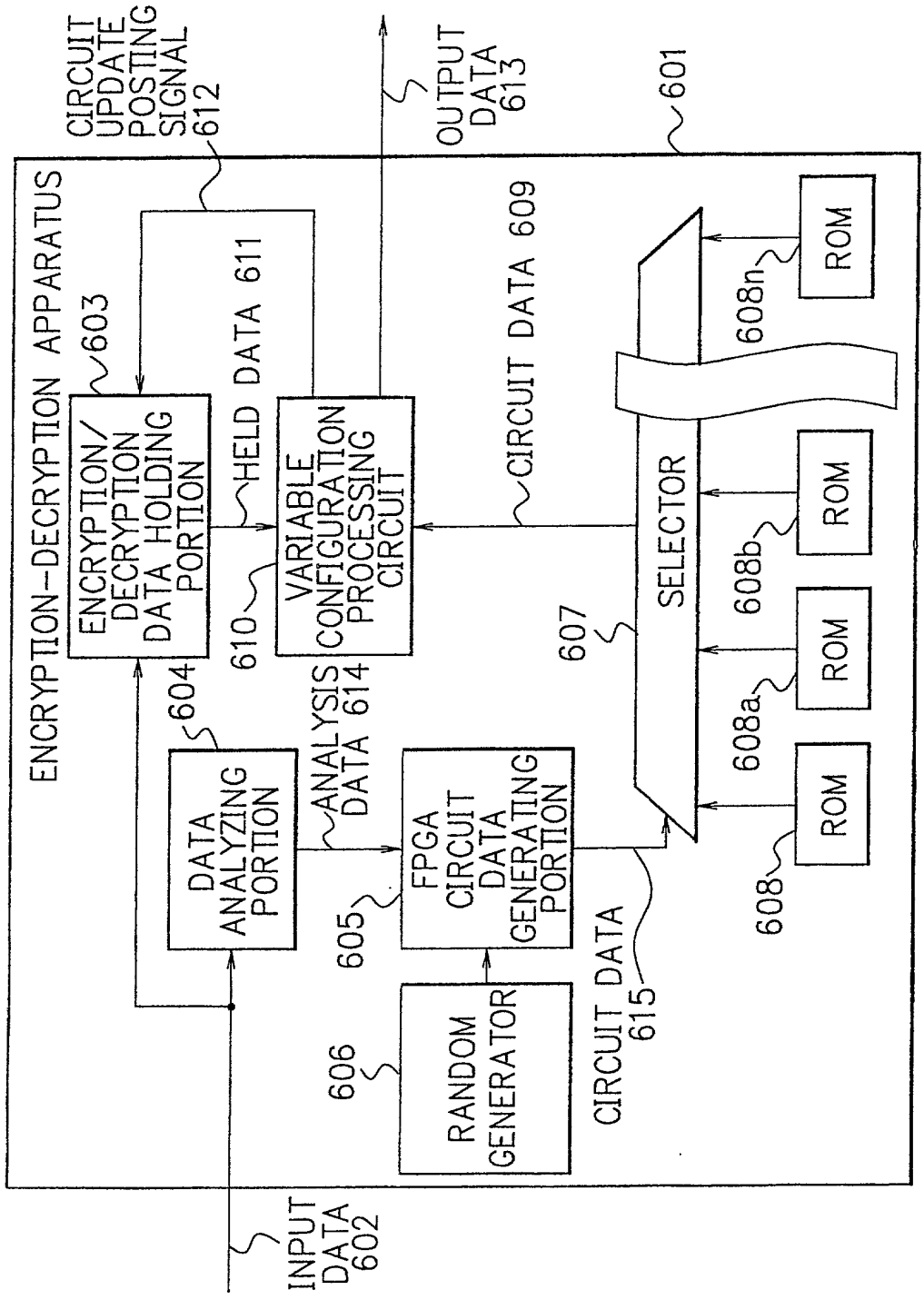

ENCRYPTION-DECRYPTION APPARATUS
601
CIRCUIT UPDATE POSTING SIGNAL 612
OUTPUT DATA 613
603
ENCRYPTION/ DECRYPTION DATA HOLDING PORTION
HELD DATA 611
610
VARIABLE CONFIGURATION PROCESSING CIRCUIT
CIRCUIT DATA 609
607
SELECTOR
608n
ROM
608b
ROM
608a
ROM
608
ROM
604
DATA ANALYZING PORTION
ANALYSIS DATA 614
605
FPGA CIRCUIT DATA GENERATING PORTION
606
RANDOM GENERATOR
CIRCUIT DATA 615
INPUT DATA 602

FIG. 9

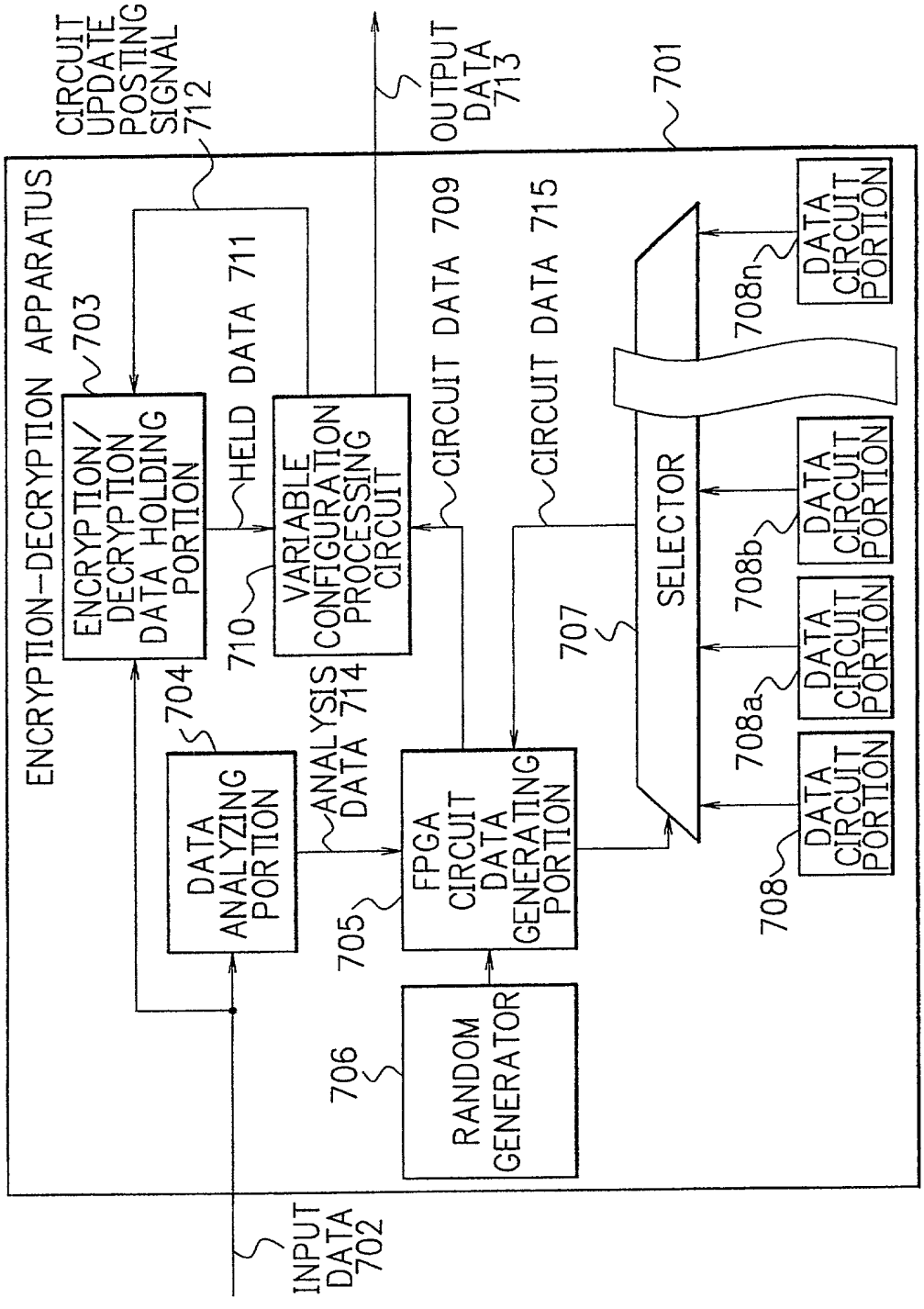

ENCRYPTION-DECRYPTION APPARATUS
701
CIRCUIT UPDATE POSTING SIGNAL 712
OUTPUT DATA 713
ENCRYPTION/ DECRYPTION DATA HOLDING PORTION
703
HELD DATA 711
VARIABLE CONFIGURATION PROCESSING CIRCUIT
710
CIRCUIT DATA 709
CIRCUIT DATA 715
DATA ANALYZING PORTION
704
ANALYSIS DATA 714
FPGA CIRCUIT DATA GENERATING PORTION
705
707
SELECTOR
RANDOM GENERATOR
706
INPUT DATA 702
708
708a
708b
708n
DATA CIRCUIT PORTION

FIG. 10

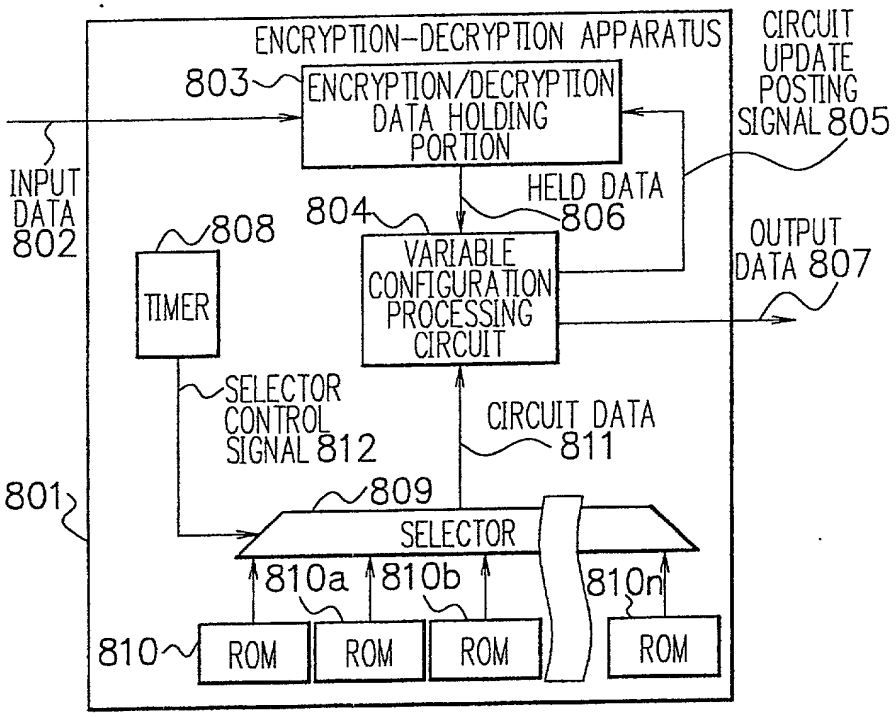


FIG. 11

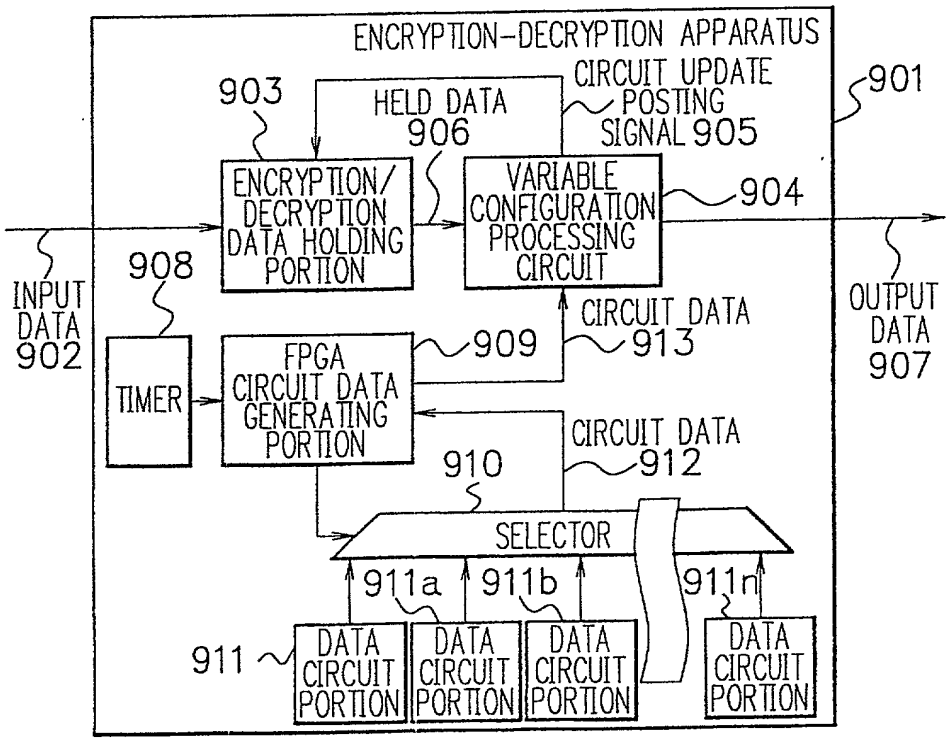


FIG. 12

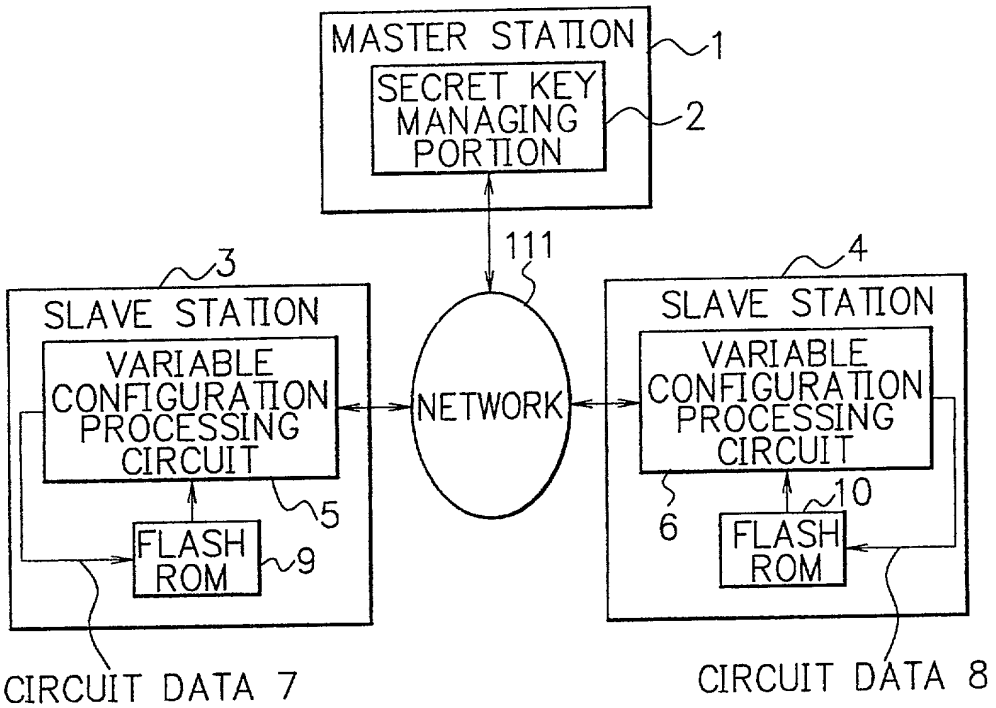
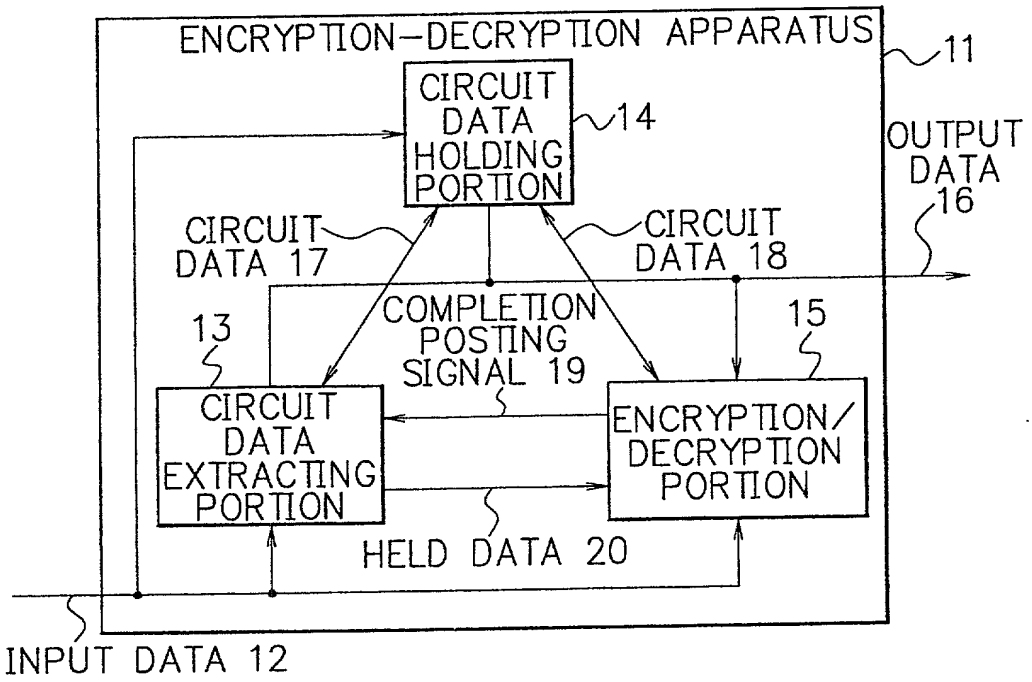

MASTER STATION
1
SECRET KEY MANAGING PORTION
2
111
3
SLAVE STATION
VARIABLE CONFIGURATION PROCESSING CIRCUIT
5
FLASH ROM
9
NETWORK
4
SLAVE STATION
VARIABLE CONFIGURATION PROCESSING CIRCUIT
6
10
FLASH ROM
CIRCUIT DATA 7
CIRCUIT DATA 8

FIG. 13


ENCRYPTION-DECRYPTION APPARATUS
11
CIRCUIT DATA HOLDING PORTION
14
OUTPUT DATA
16
CIRCUIT DATA 17
CIRCUIT DATA 18
13
COMPLETION POSTING SIGNAL 19
15
CIRCUIT DATA EXTRACTING PORTION
ENCRYPTION/ DECRYPTION PORTION
HELD DATA 20
INPUT DATA 12